and 9(c) show an expanded detail of the overlaid waveforms. Figures 8(b) and 8(c) also show a voltage waveform Op4, and

Please replace the paragraph on page 11, beginning at line 11 through line 17, with the following:

Figure 10 shows a further embodiment of the invention in which inverted gate means in the form of a NOT gate U4 is used as a fast switching comparator. The switching level of the gate can vary appreciably with time and temperature; however, this can be controlled by provision of a further negative DC feedback path connected between the output of NOT gate U4 and the control input i.e. the gate of FET Q1. To this end, a simple, single RC low pass filter (R_5,C_5) provides sufficient filtering to establish the mean output level. In this way, the NOT gate U4 is automatically 'self-biased' to the correct switching level.

IN THE CLAIMS:

Please replace claims 1-2, 6, 12-13, 27, and 30 with the following:

1. (Amended) An anti-jitter circuit for reducing time jitter in an input pulse train comprising:

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means,

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